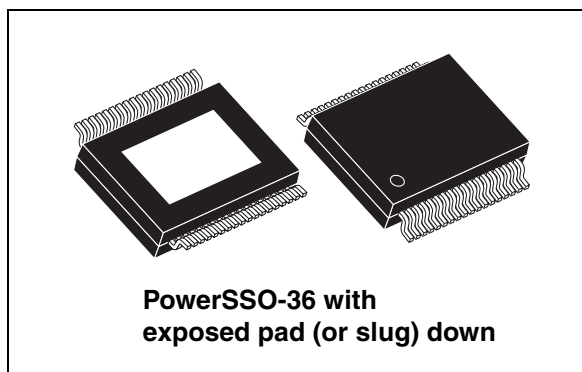


## 25 W mono BTL class-D audio amplifier

### Features

- 20 W continuous output power:  
 $R_L = 8 \Omega$ , THD = 10% at  $V_{CC} = 18 V$
- 25 W continuous output power:  
 $R_L = 6 \Omega$ , THD = 10% at  $V_{CC} = 16 V$
- Wide range single supply operation (5 V - 18 V)
- High efficiency ( $\eta = 90\%$ )
- Four selectable, fixed gain settings of 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- No 'pop' at turn-on/off
- Standby and mute features
- Short circuit protection
- Thermal overload protection
- Externally synchronizable



### Description

The TDA7491MV is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and slug-down package no heatsink is required.

Furthermore, the filterless operation allows a reduction in the external component count.

TDA7491MV is pin to pin compatible to TDA7491LP, TDA7491P, TDA7491HV (please refer to [Application circuit on page 15](#) for further details).

**Table 1. Device summary**

Order codes	Operating Temp. range	Package	Packing
TDA7491MV	0 °C to 70 °C	PowerSSO-36 (slug down)	Tube
TDA7491MV13TR	0 °C to 70 °C	PowerSSO-36 (slug down)	Tape and reel

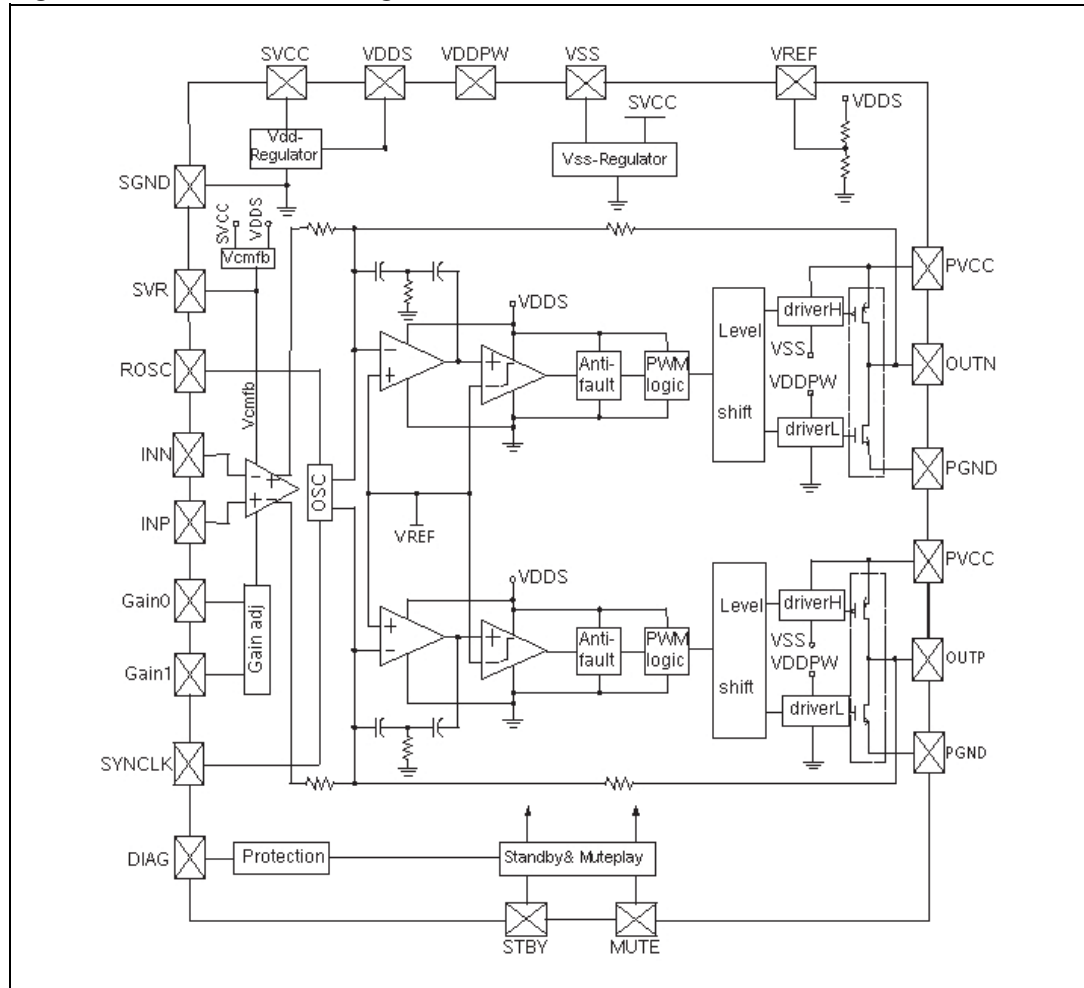
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# 1 Device block diagram

Figure 1 shows the TDA7491MV block diagram.

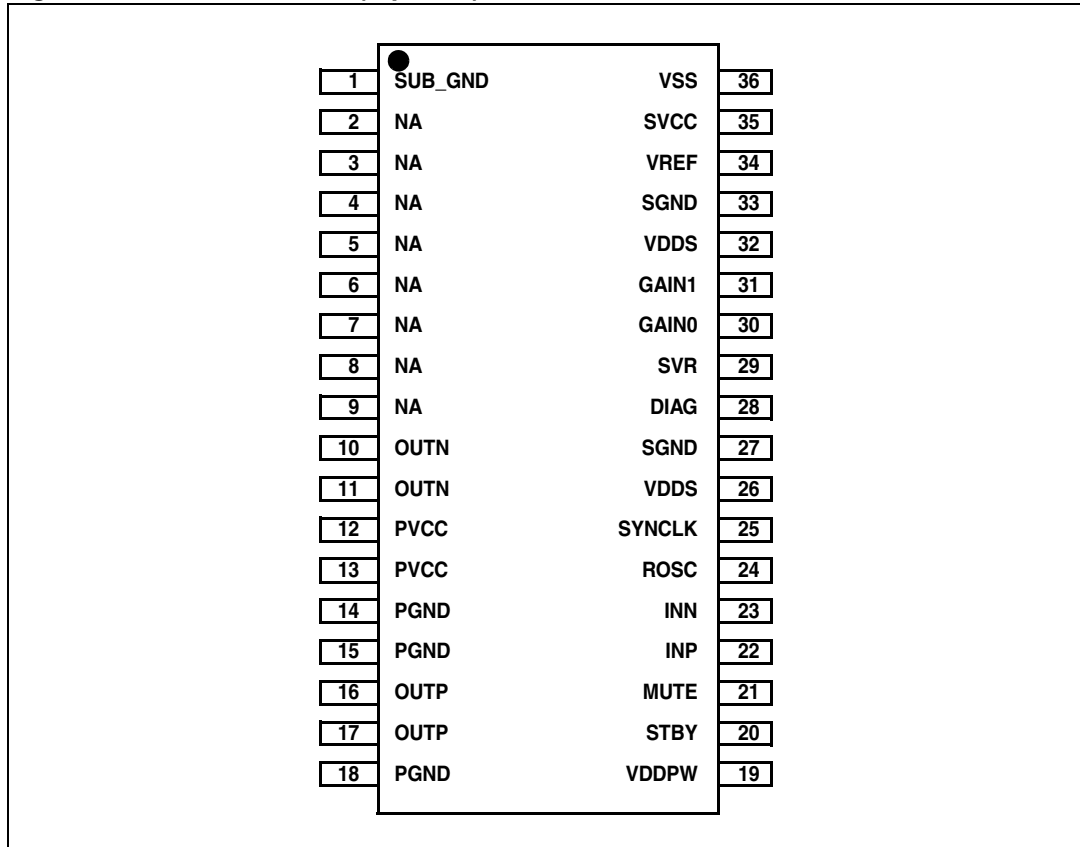
Figure 1. Internal block diagram



## 2 Pin description

### 2.1 Pin-out

Figure 2. Pin connection (top view)



## 2.2 Pin list

**Table 2. Pin description list**

Number	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	NA	NA	NA
4,5	NA	NA	NA
6,7	NA	NA	NA
8,9	NA	NA	NA
10,11	OUTNA	OUT	Negative PWM output for right channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage round for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage round
19	VDDPW	OUT	3.3 V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3 V (nominal) regulator output referred to gnd for signal blocks
27	SGND	POWER	Signal Ground
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	VDDS	POWER	To be connected to VDD signal
33	SGND	POWER	Signal Ground
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3 V (nominal) regulator output referred to power supply

### 3 Electrical specifications

#### 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
VCC	DC supply voltage for pins PVCCA, PVCCB, SVCC	24	V
T <sub>op</sub>	Operating temperature	0 to 70	°C
T <sub>j</sub>	Junction temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-40 to 150	°C

#### 3.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Min.	Typ.	Max.	Unit
R <sub>th j-case</sub>	Thermal resistance, junction to case		2	3	°C/W
R <sub>th j-amb</sub>	Thermal resistance, junction to ambient (mounted on recommended PCB) <sup>(1)</sup>		24		

1. FR4 with vias to copper area of 9 cm<sup>2</sup> (see also [Section 7.9: Heatsink requirements on page 22](#)).

#### 3.3 Electrical specifications

Unless otherwise stated, the results in [Table 5](#) below are given for the conditions: VCC = 18 V, R<sub>L</sub> (load) = 8 Ω, R<sub>OSC</sub> = 39 kΩ, C1 = 100 nF, f = 1 kHz, G<sub>V</sub> = 20 dB, and Tamb = 25 °C.

**Table 5. Electrical specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC	Supply voltage for pins PVCCA, PVCCB, SVCC		5		18	V
I <sub>q</sub>	Total quiescent			26	35	mA
I <sub>qSTBY</sub>	Quiescent current in standby			2.5	5.0	μA
V <sub>OS</sub>	Output offset voltage	Play mode	-150		150	mV
V <sub>OS</sub>	Output offset voltage	Mute mode	-60		60	mV
I <sub>OC</sub>	Over current protection threshold	R <sub>L</sub> = 0 Ω	3	5		A
T <sub>j</sub>	Junction temperature at thermal shut-down			150		°C
R <sub>i</sub>	Input resistance	Differential input	55	60		kΩ
V <sub>Ov</sub>	Over voltage protection threshold		19	21		

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R <sub>dsON</sub>	Power transistor on resistance	High side		0.2		Ω
		Low side		0.2		
P <sub>o</sub>	Output power	THD = 10%		20		W
		THD = 1%		16		
P <sub>o</sub>	Output power	R <sub>L</sub> = 8 Ω, THD = 10% VCC=12V		9.5		W
		R <sub>L</sub> = 8 Ω, THD = 1% VCC = 12 V		7.2		
P <sub>o</sub>	Output power	R <sub>L</sub> = 6 Ω, THD = 10% VCC=16V		20		W
		R <sub>L</sub> = 6 Ω, THD = 1% VCC = 16 V		16		
P <sub>D</sub>	Dissipated power	P <sub>o</sub> = 20 W + 20 W, THD = 10%		4.0		W
η	Efficiency	P <sub>o</sub> = 20 W + 20 W	80	90		%
THD	Total harmonic distortion	P <sub>o</sub> = 1 W		0.1	0.4	%
G <sub>V</sub>	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
ΔG <sub>V</sub>	Gain matching		-1		1	dB
CT	Cross talk	f = 1 kHz		50		dB
eN	Total input noise	A Curve, G <sub>V</sub> = 20 dB		20		μV
		f = 22 Hz to 22 kHz		25	35	
SVRR	Supply voltage rejection ratio	Fr = 100 Hz, Vr = 0.5 V, C <sub>SVR</sub> = 10 μF	40	50		dB
T <sub>r</sub> , T <sub>f</sub>	Rise and fall times			50		ns
F <sub>SW</sub>	Switching frequency	Internal oscillator	290	310	330	kHz
F <sub>SWR</sub>	Output switching frequency	With internal oscillator <sup>(1)</sup>	250			kHz
		With external oscillator <sup>(2)</sup>	250			
V <sub>inH</sub>	Digital input high (H)		2.3			V
V <sub>inL</sub>	Digital input low (L)				0.8	
Function mode	Standby, mute and play modes	STBY < 0.5 V, MUTE = X	Standby			
		STBY > 2.5 V, MUTE < 1 V	Mute			
		STBY > 2.5 V, MUTE > 2 V	Play			
A <sub>MUTE</sub>	Mute attenuation	VMute = 1 V	60	80		dB

1.  $F_{SW} = 10^6 / (64 * R_{OSC} + 440)$  kHz,  $f_{SYNCLK} = 2 * F_{SW}$  with R1 = 3 kΩ (see [Figure 17](#)).

2.  $F_{SW} = f_{SYNCLK} / 2$  with the frequency of the external oscillator.

# 4 Characterization curves

Figure 3. Output power vs supply voltage

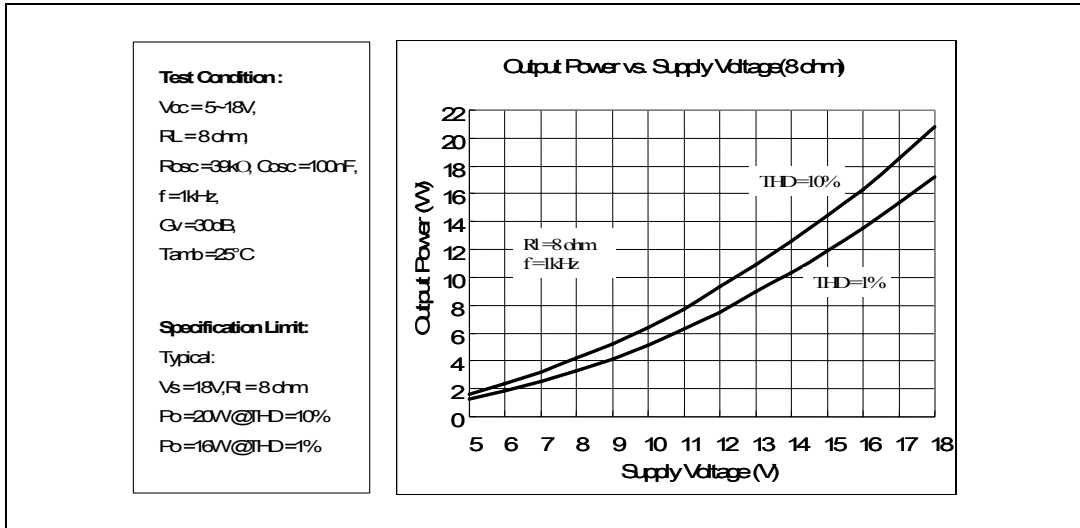


Figure 4. THD vs output power (1 kHz)

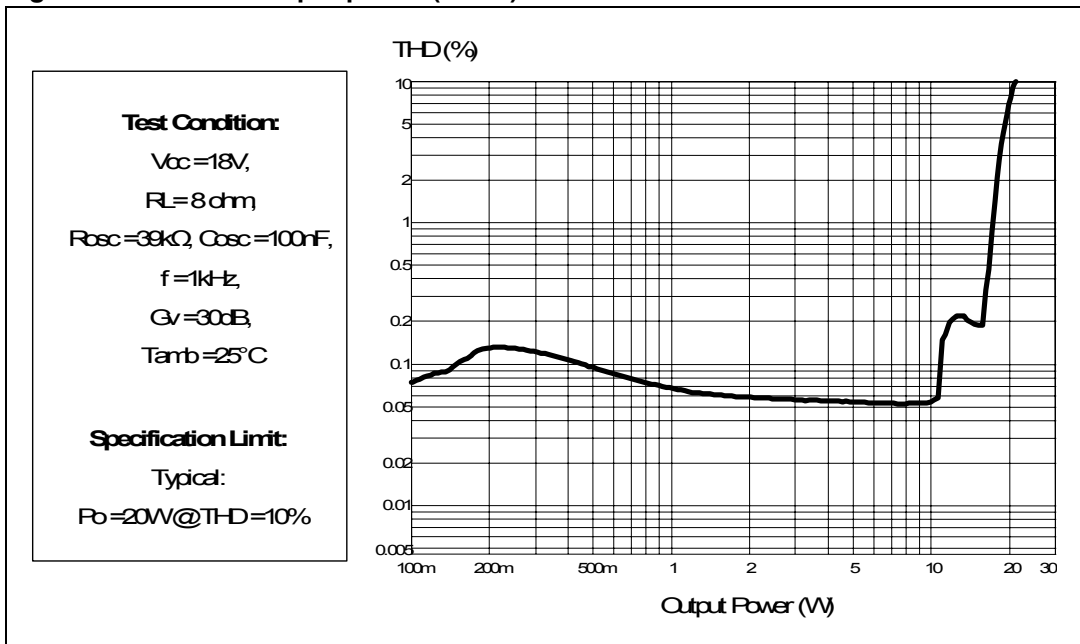




Figure 5. THD vs output power (100 Hz)

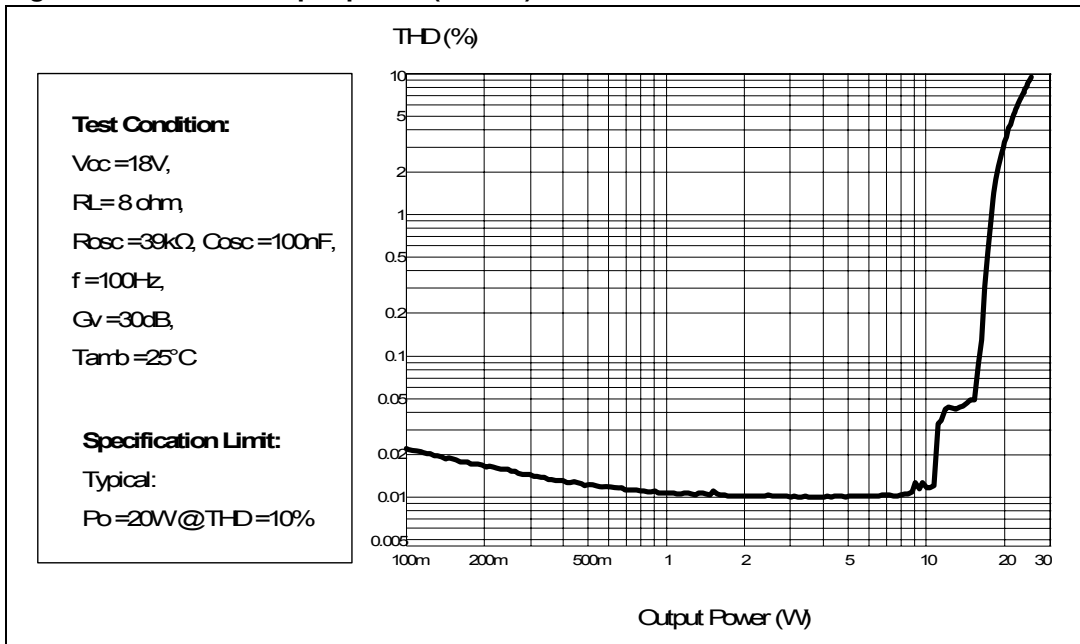


Figure 6. THD vs Frequency

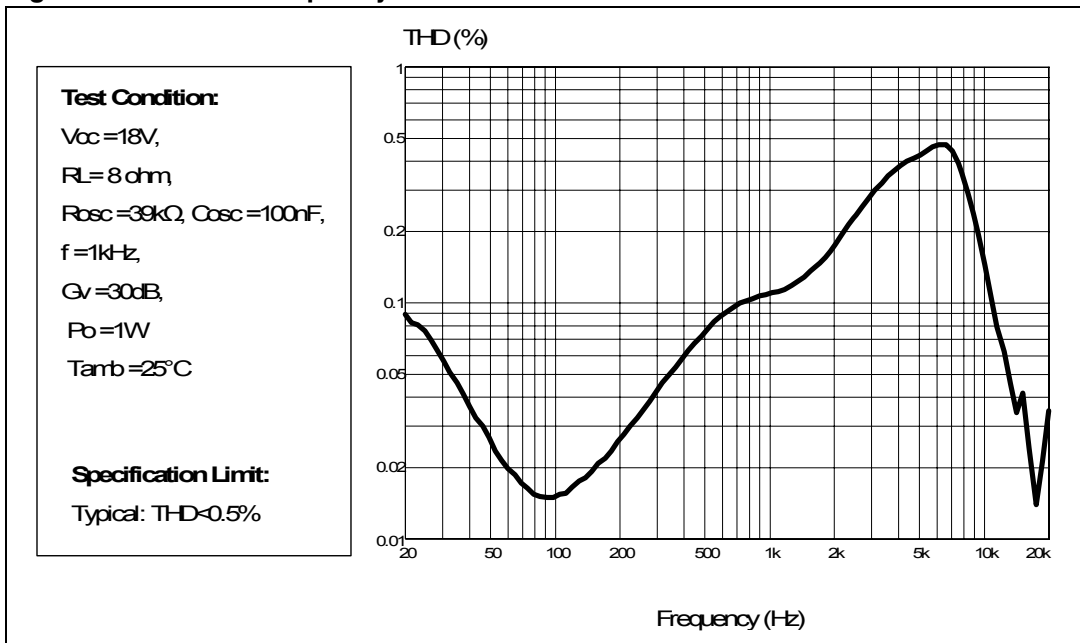


Figure 7. Frequency Response

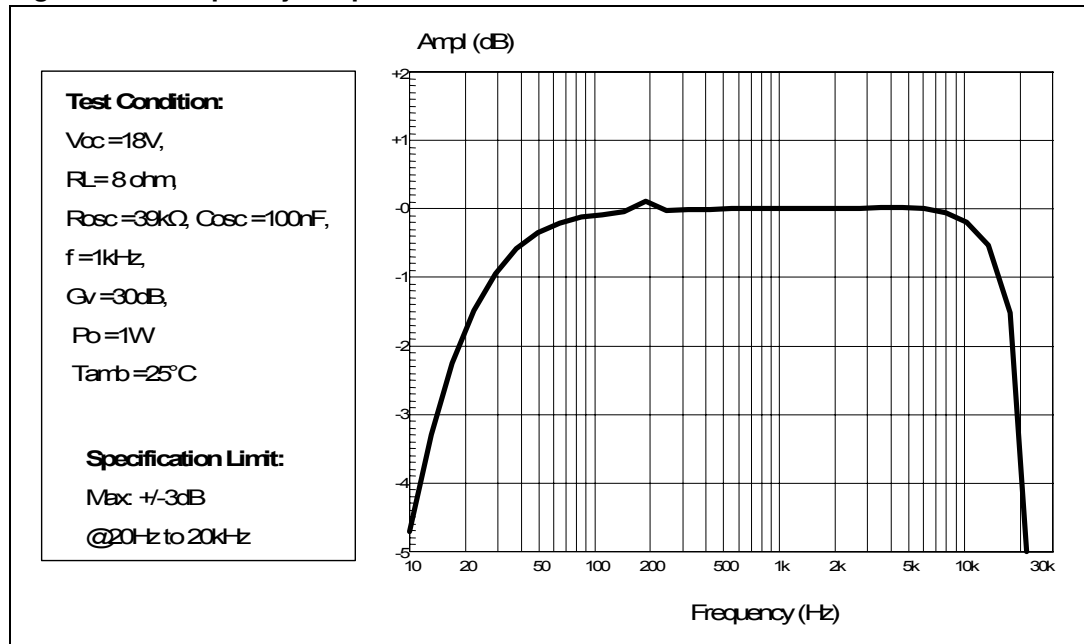


Figure 8. FFT (0 dB)

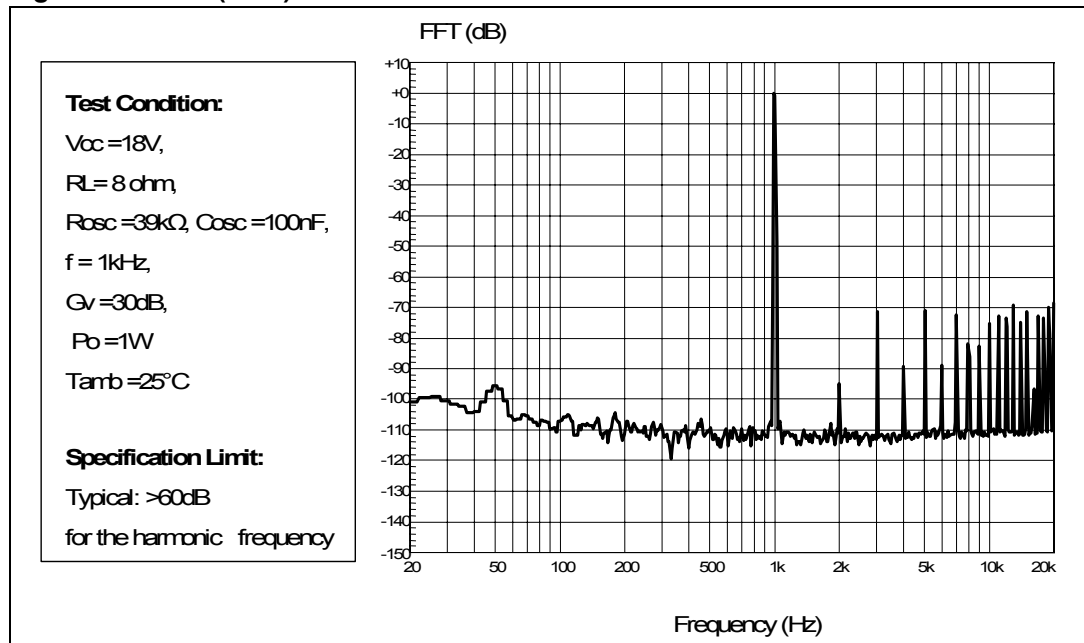


Figure 9. FFT (-60 dB)

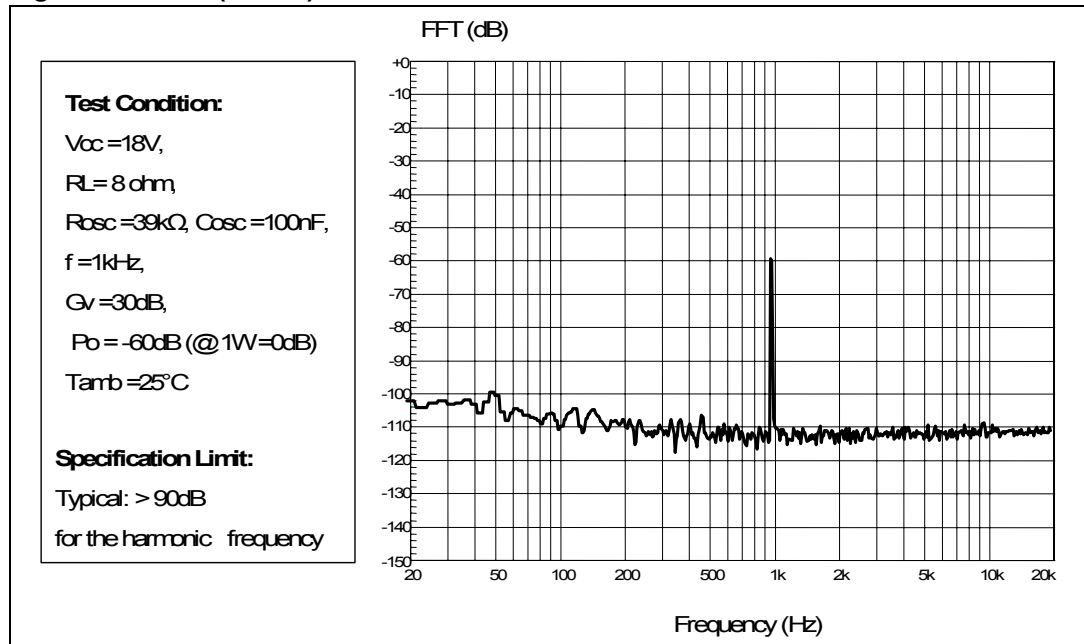


Figure 10. Closed-loop gain vs frequency

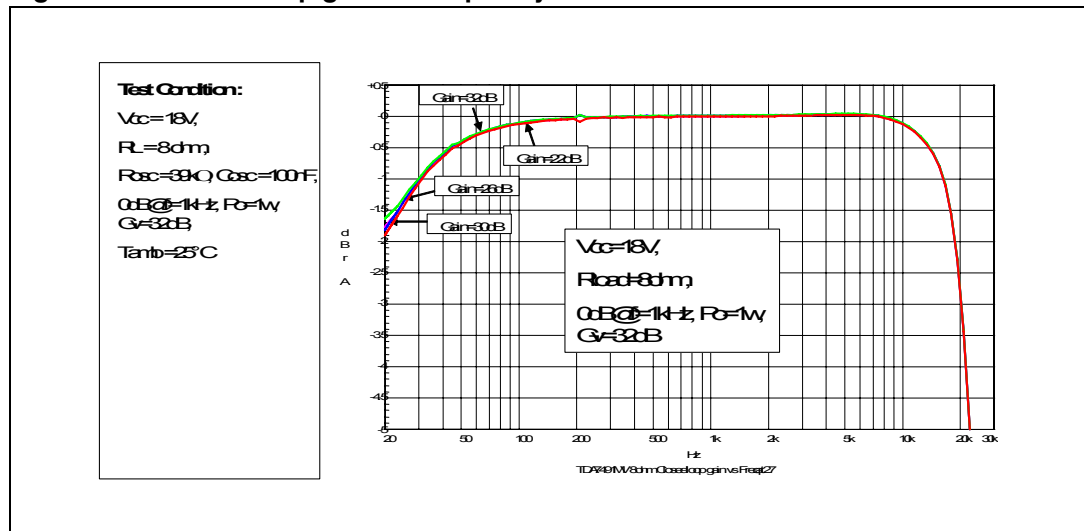


Figure 11. Power dissipation and efficiency vs output power

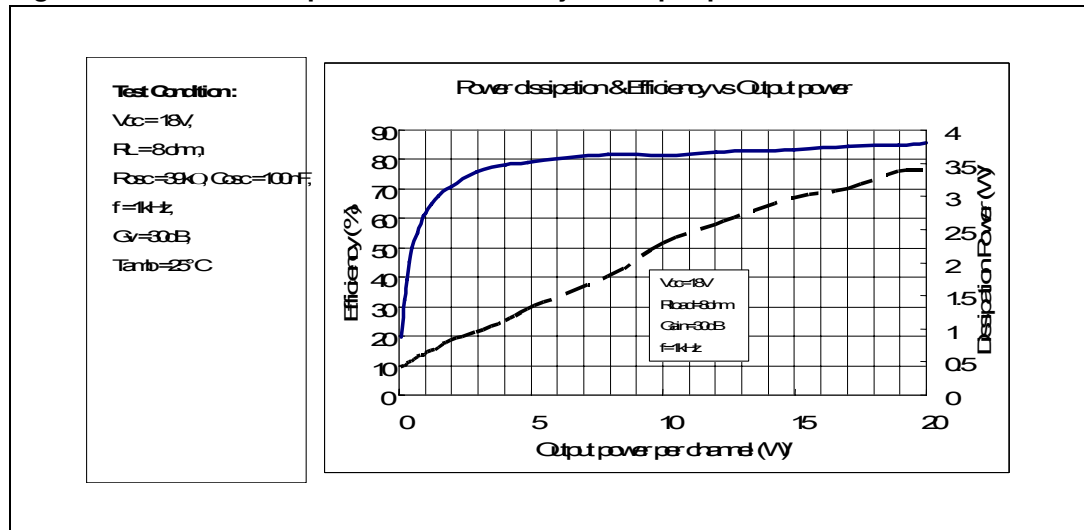


Figure 12. Attenuation vs mute voltage

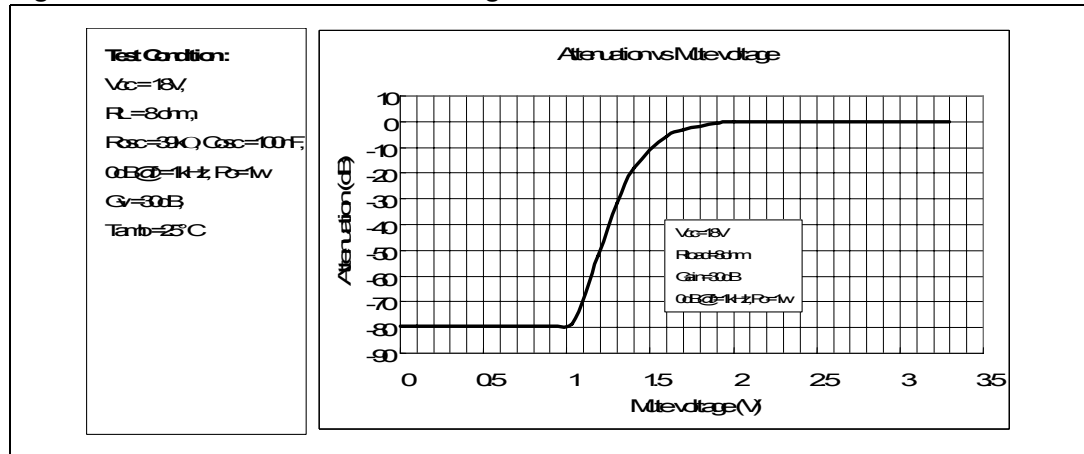


Figure 13. Current consumption vs voltage on pin STBY

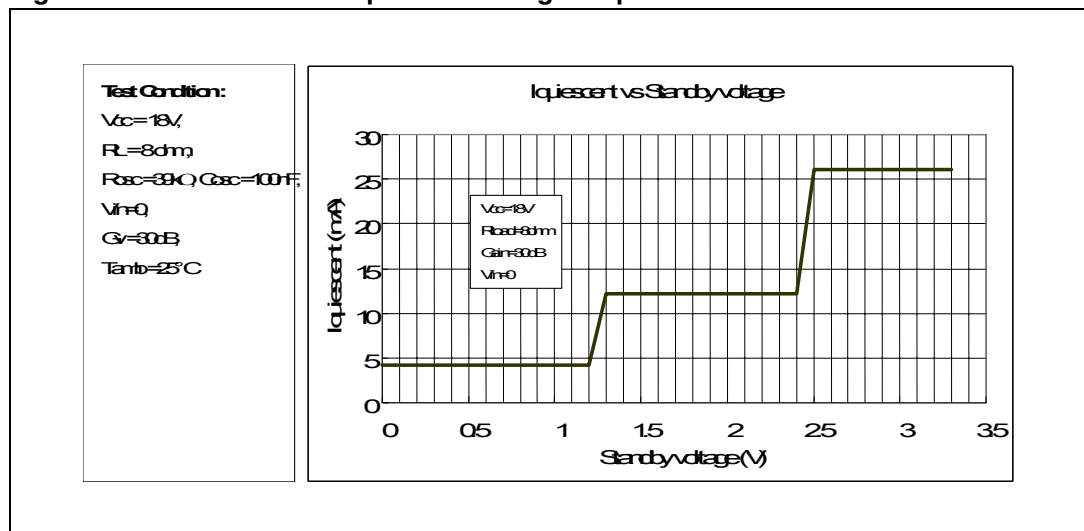


Figure 14. Attenuation vs voltage on pin STBY

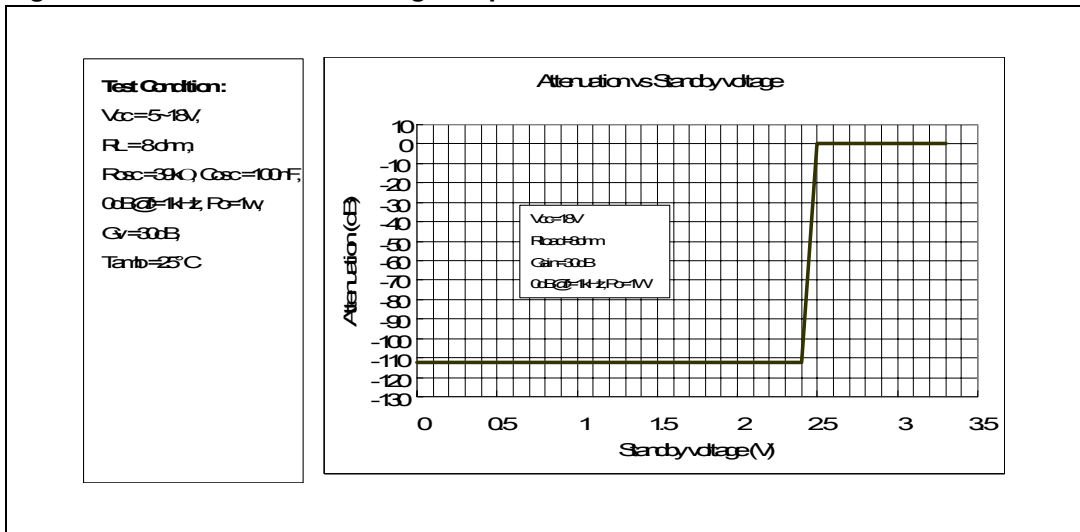
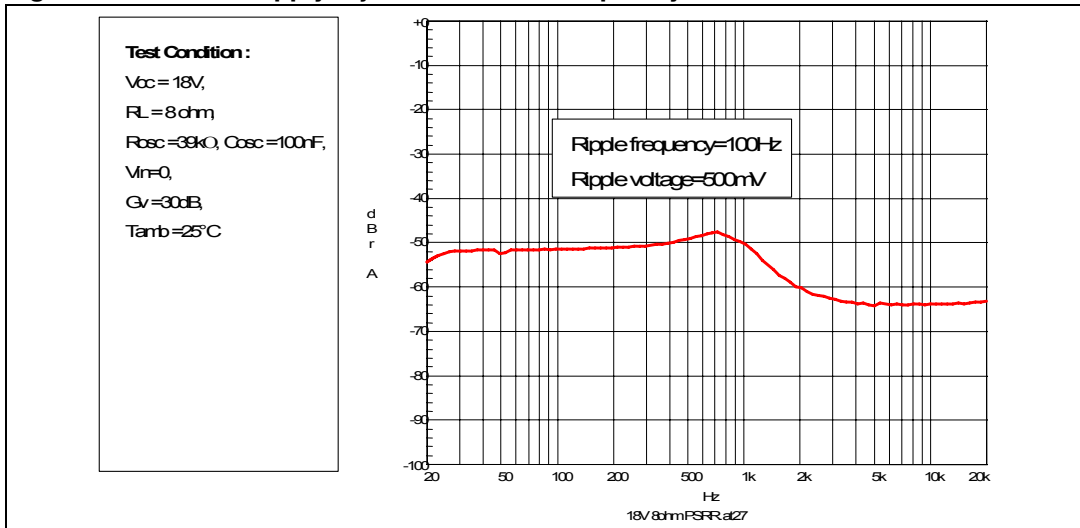


Figure 15. Power supply rejection ratio vs frequency

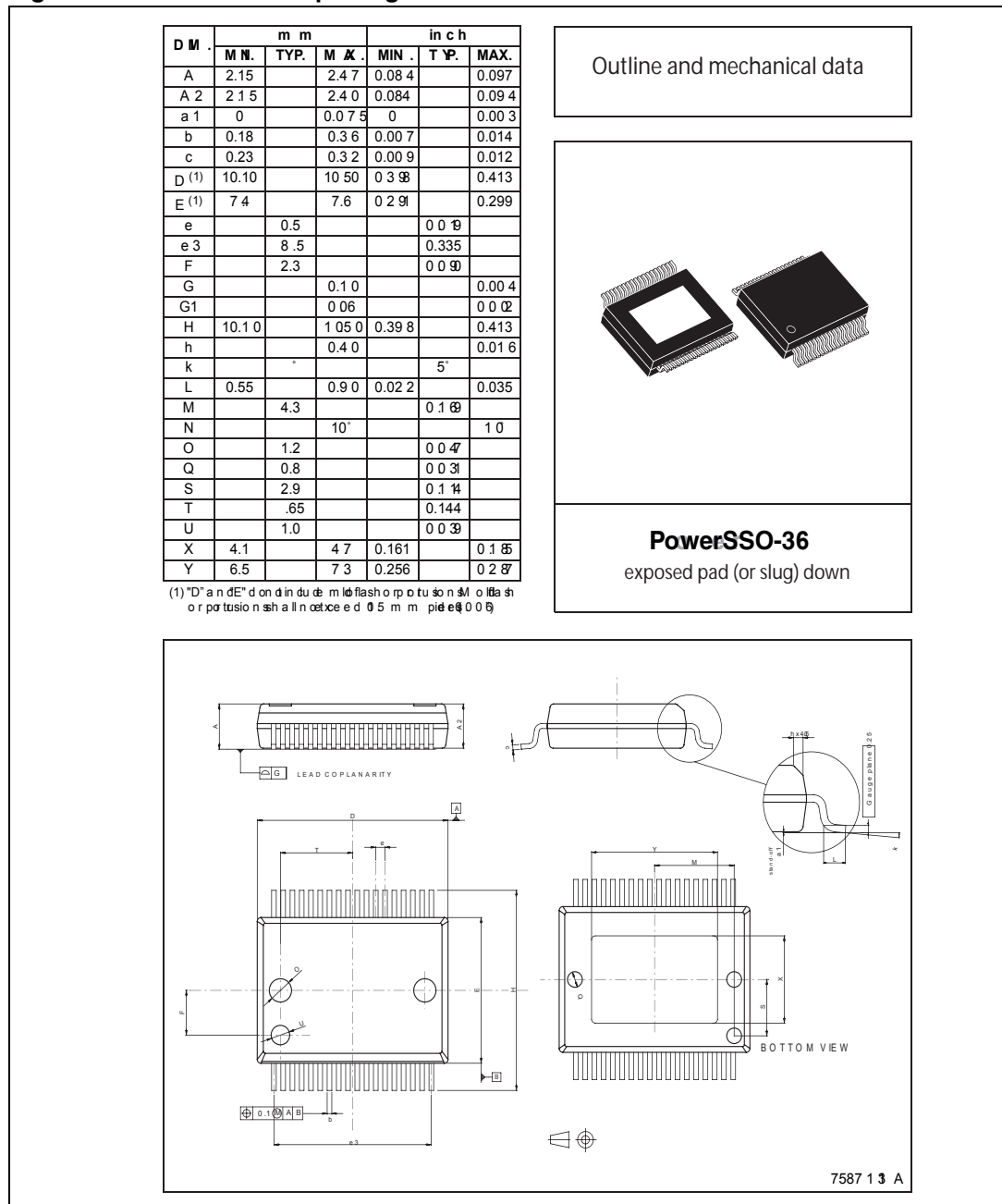


# 5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

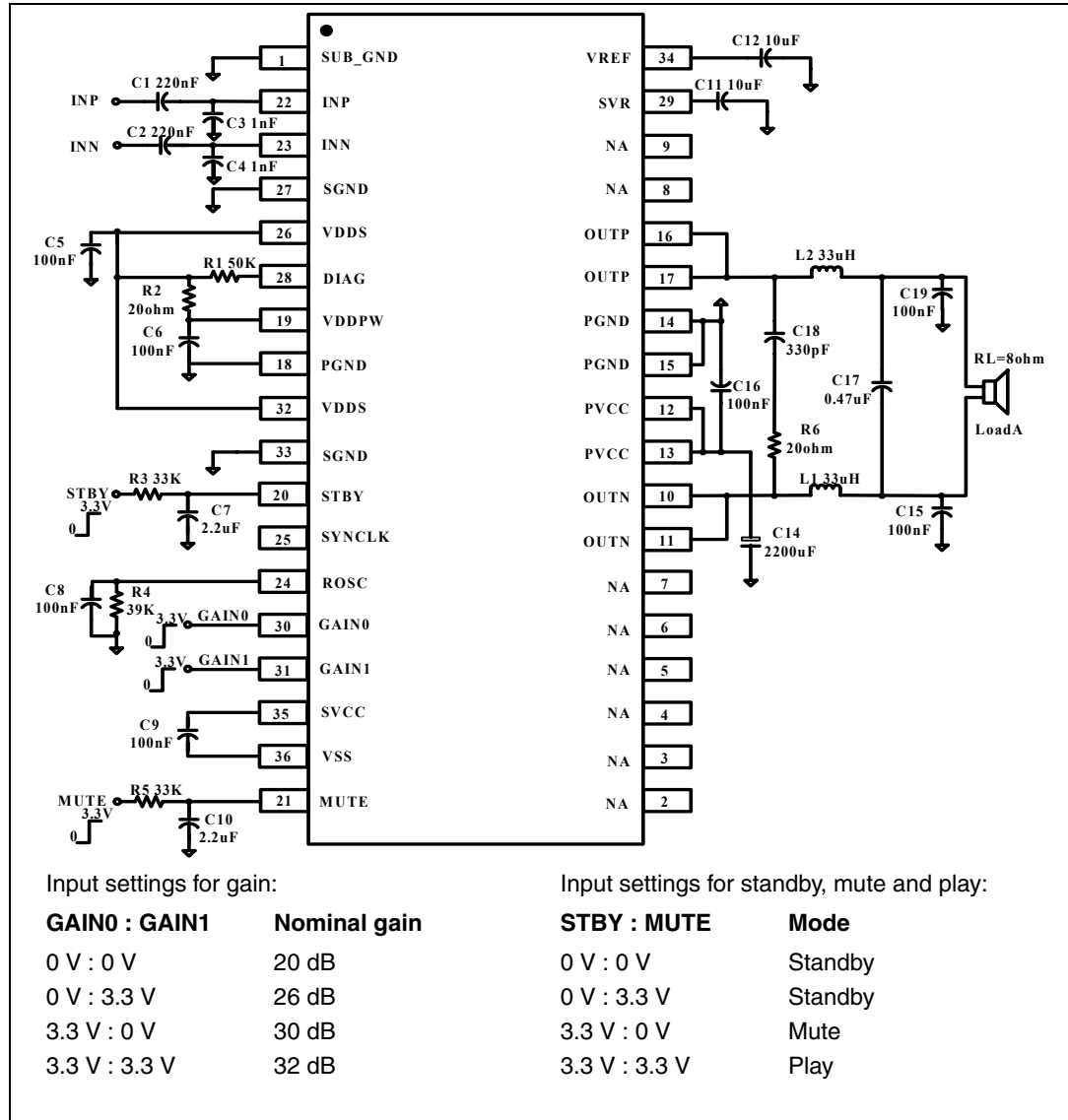
ECOPACK specifications are available at: <http://www.st.com>.

**Figure 16. PowerSSO-36 package dimensions**



## 6 Application circuit

Figure 17. Application circuit



### 6.1 Compatibility with TDA7491 stereo analog class D BTL family

TDA7491MV mono BTL analog class D is derived from the TDA7491 stereo analog class D BTL family. TDA7491MV does not have the right channel of the stereo BTL family.

Moving the application from stereo to mono, in order to guarantee the pin to pin compatibility it is necessary to connect the right channel inputs (pins 32 and 33 of TDA7491 BTL family) to Vcc and GND (pin 32 to SVCC and pin 33 to GNDS).

# 7 Application information

## 7.1 Mode selection

The three operating modes of the TDA7491MV are set by the two inputs STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

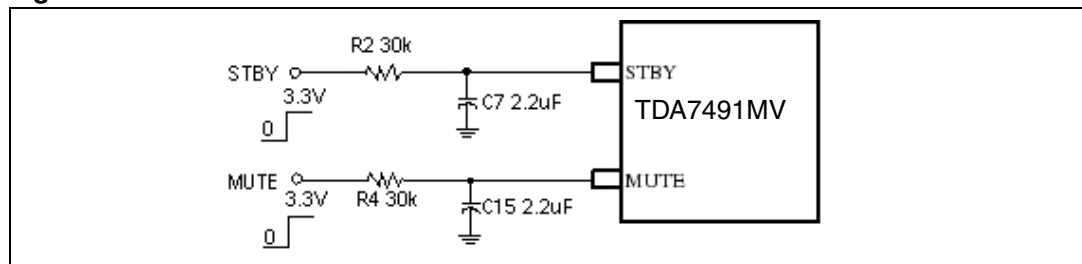
The protection functions of the TDA7491MV are realized by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 18*. The input current of the corresponding pins must be limited to 200  $\mu$ A.

**Table 6. Mode settings**

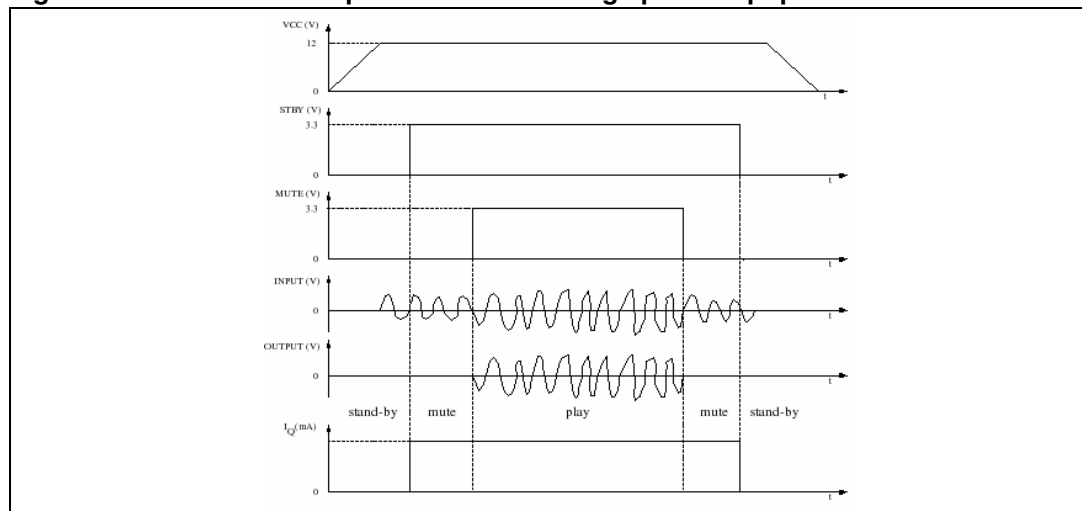
Mode Selection	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in *Table 5: Electrical specifications on page 6*

**Figure 18. STBY and MUTE circuit**



**Figure 19. Turn on/off sequence for minimizing speaker “pop”**





## 7.2 Gain setting

The gain of the TDA7491MV is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

**Table 7. Gain settings**

GAIN0	GAIN1	Nominal gain, $G_v$ (dB)
0	0	20
0	1	26
1	0	30
1	1	32

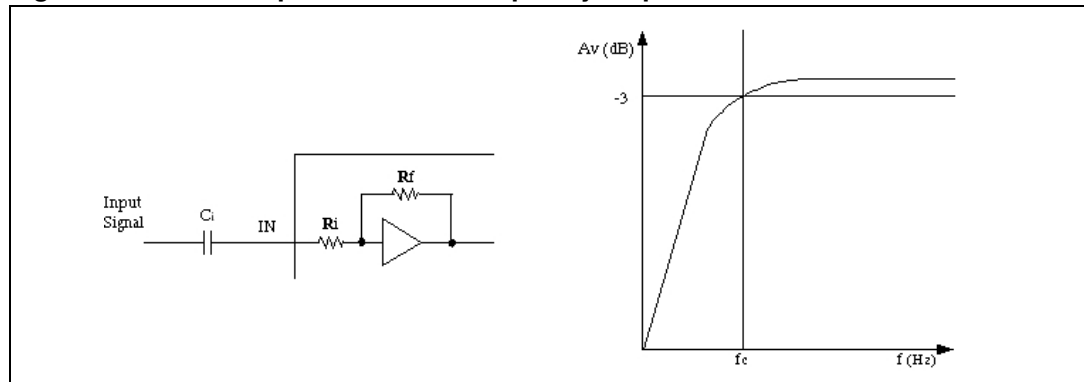
## 7.3 Input resistance and capacitance

The input impedance is set by an internal resistor  $R_i = 60\text{ k}\Omega$  (typical). An input capacitor ( $C_i$ ) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in [Figure 20](#). For  $C_i = 220\text{ nF}$  the high-pass filter cut-off frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

**Figure 20. Device input circuit and frequency response**



## 7.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7491MV as master clock, while the other devices are in slave mode (that is, externally clocked). The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

### 7.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency,  $F_{SW}$ , is controlled by the resistor,  $R_{OSC}$ , connected to pin ROSC:

$$F_{SW} = 10^6 / (64 * R_{OSC} + 440) \text{ kHz}$$

where  $R_{OSC}$  is in  $k\Omega$

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$F_{SYNCLK} = 2 * F_{SW}$$

For master mode to operate correctly then resistor  $R_{OSC}$  must be less than 60  $k\Omega$  as given below in [Table 8](#).

### 7.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in [Table 8](#).

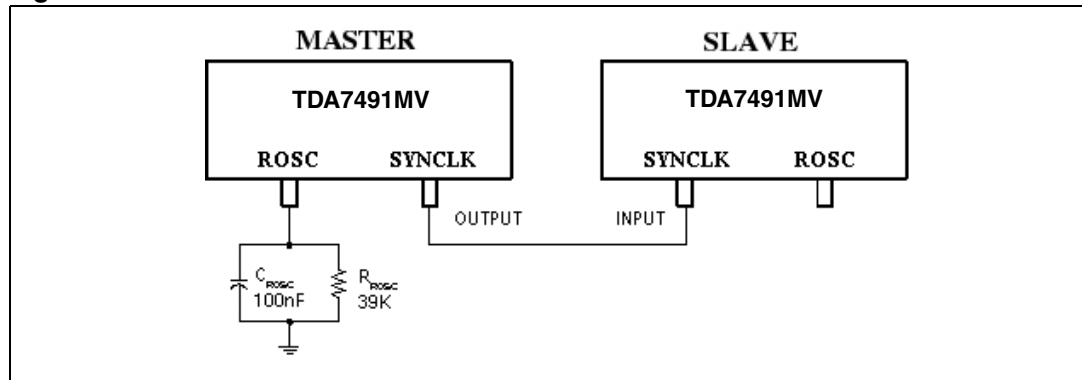
The output switching frequency of the slave devices is:

$$F_{SW} = F_{SYNCLK} / 2$$

**Table 8. How to set up SYNCLK**

Mode	ROSC	SYNCLK
Master	$R_{OSC} < 60 \text{ k}\Omega$	OUTPUT
Slave	Floating (not connected)	INPUT

**Figure 21. Master and Slave Connection**



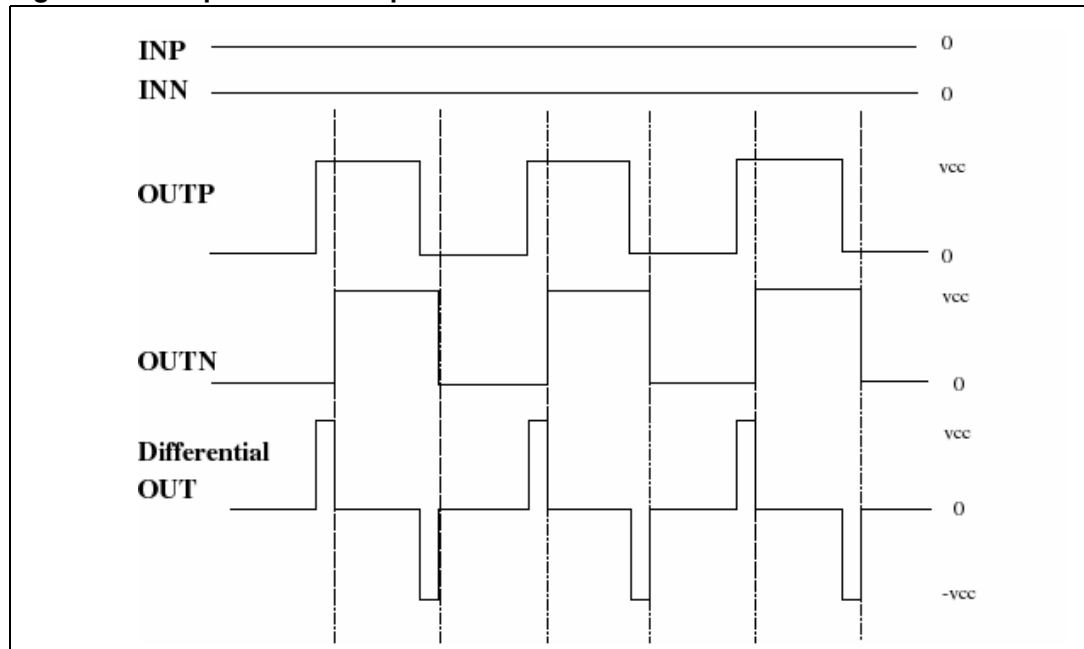
## 7.5 Filterless modulation

The output modulation scheme of the BTL is called unipolar pulse width modulation (PWM). The differential output voltages change between zero and +Vcc and between zero and -Vcc. This is in contrast to the traditional bipolar PWM outputs which change between +Vcc and -Vcc.

An advantage of this scheme is that it effectively doubles the switching frequency of the differential output waveform. The OUTP and OUTN are in the same phase when the input is zero, then the switching current is low and the loss in the load is small. In practice, a short delay is introduced between these two outputs in order to avoid the BTL output switching at the same time.

TDA7491MV can be used without a filter before the speaker, because the frequency of the TDA7491MV output is beyond the audio frequency, the audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

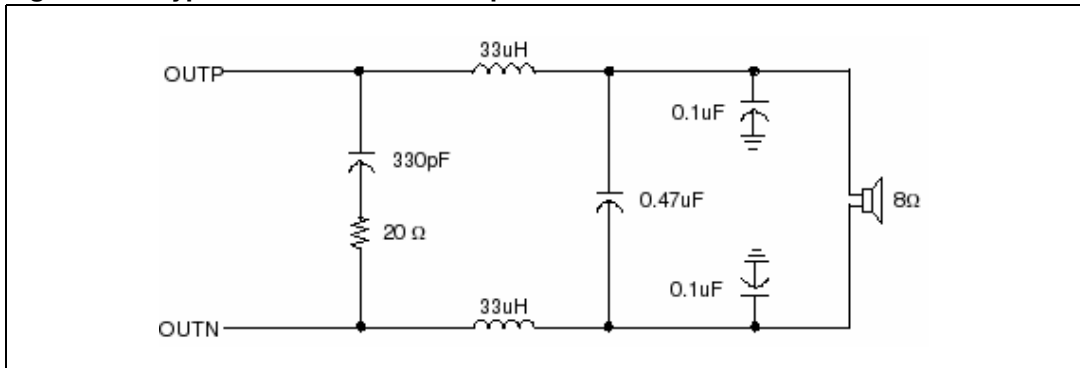
**Figure 22. Unipolar PWM output**



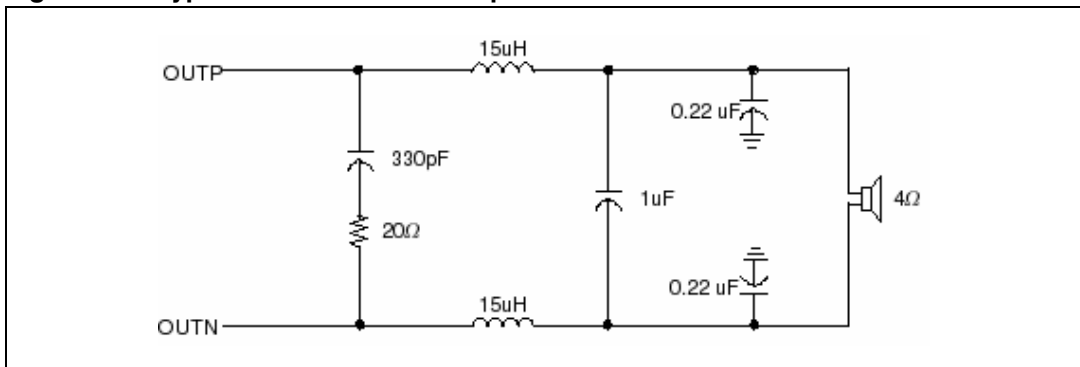
### 7.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in [Figure 23](#) and [Figure 24](#) below.

**Figure 23. Typical LC filter for a 8-Ω speaker**



**Figure 24. Typical LC filter for a 4-Ω speaker**



## 7.7 Protection function

The TDA7491MV is fully protected against over-voltages, under-voltages, over-currents and thermal overloads as explained here. See also [Table 5: Electrical specifications on page 6](#).

### Overvoltage protection (OVP)

If the supply voltage exceeds 20 V (nominal) the over-voltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

### Undervoltage protection (UVP)

If the supply voltage drops below 4 V (nominal) the under-voltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

### Overcurrent protection (OCP)

If the output current exceeds 4 A (nominal) the over-current protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the over-current condition is still present then the OCP remains active. The restart time,  $T_{OC}$ , is determined by the R-C components connected to pin STBY.

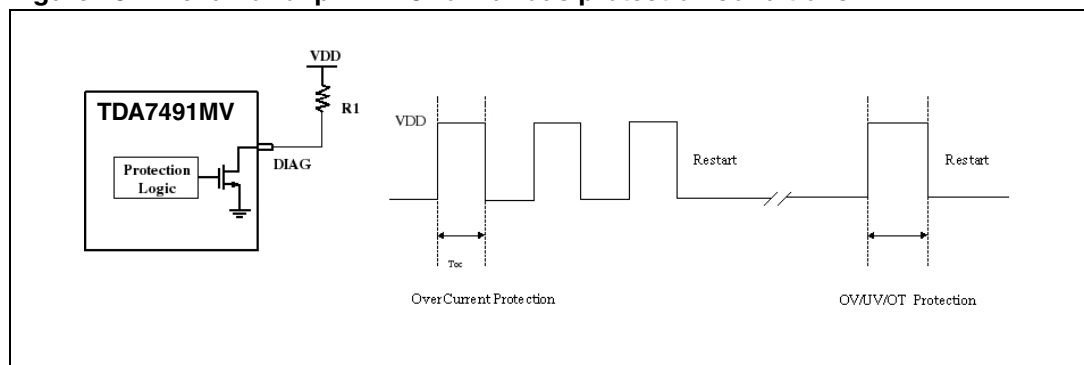
### Thermal protection (OTP)

If the junction temperature,  $T_j$ , reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. At  $T_j = 155$  °C (nominally), the device shuts down and the output is forced to the high impedance state. When the device cools sufficiently the device restarts.

## 7.8 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (< 20 V) by a pull-up resistor whose value is limited by the maximum sinking current (200  $\mu$ A) of the pin.

**Figure 25. Behavior of pin DIAG for various protection conditions**



### 7.9 Heatsink requirements

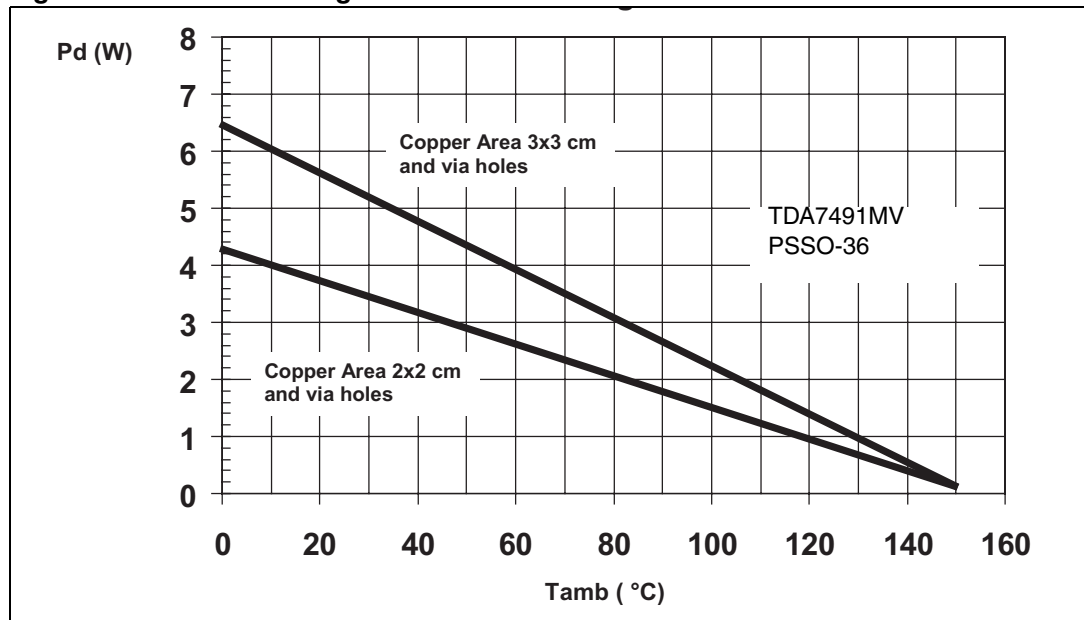
A thermal resistance of 24 °C/W can be obtained using the PCB copper ground layer with 16 vias connecting it to the contact area for the slug. Ensure that the copper ground area is a nominal 9 cm<sup>2</sup> for 24 °C/W.

Figure 26 shows the derating curves for copper areas of 4 cm<sup>2</sup> and 9 cm<sup>2</sup>.

As with most amplifiers, the power dissipated within the device depends primarily on the supply voltage, the load impedance and the output modulation level.

The maximum estimated power dissipation for the TDA7491MV is less than 4 W. When properly mounted on the above PCB the junction temperature could increase by 96 °C. However, with a musical program the dissipated power is about 40% less, leading to a temperature increase of around 60 °C. Even at the maximum recommended ambient temperature for consumer applications of 50 °C there is still a clear safety margin before the maximum junction temperature (150 °C) is reached.

Figure 26. Power derating curves for PCB used as heatsink



## 8 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
21-Oct-2008	1	Initial release.

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